8051 INSTRUCTION SET

NOTES ON INSTRUCTION SET AND ADDRESSING MODES

Rn Register R7-R0 of the currently selected Register Bank.
direct 8-bit internal data location's address. This could be an Internal Data RAM location (0-127) or a SFR [i.e., I/O port, control register, status register, etc. (128-255)].
@Ri 8-bit internal data RAM location (0-255) addressed indirectly through register R1 or R0.
#data 8-bit constant included in the instruction.
#data 16 16-bit constant included in the instruction
addr 16 16-bit destination address. Used by LCALL and LJMP. A branch can be anywhere within the 64k-byte Program Memory address space.
addr 11 11-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2k-byte page of program memory as the first byte of the following instruction.
rel Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is –128 to +127 bytes relative to first byte of the following instruction.
bit Direct Addressed bit in Internal Data RAM or Special Function Register.

ARITHMETIC OPERATIONS		Byte	Oscillator Period
ADD A,Rn	Add register to Accumulator	1	12
ADD A,direct	Add direct byte to Accumulator	2	12
ADD A,@Ri	Add indirect RAM to Accumulator	1	12
ADD A,#data	Add immediate data to Accumulator	2	12
ADDC A,Rn	Add register to Accumulator with carry	1	12
ADDC A,direct	Add direct byte to Accumulator with carry	2	12
ADDC A,@Ri	Add indirect RAM to Accumulator with carry	1	12
ADDC A,#data	Add immediate data to ACC with carry	2	12
SUBB A,Rn	Subtract Register from ACC with borrow	1	12
SUBB A,direct	Subtract direct byte from ACC with borrow	2	12
SUBB A,@Ri	Subtract indirect RAM from ACC with borrow	1	12
SUBB A,#data	Subtract immediate data from ACC with borrow	2	12
INC A	Increment Accumulator	1	12
INC Rn	Increment register	1	12
INC direct	Increment direct byte	2	12
INC @Ri	Increment indirect RAM	1	12
DEC A	Decrement Accumulator	1	12
DEC Rn	Decrement Register	1	12
DEC direct	Decrement direct byte	2	12
DEC @Ri	Decrement indirect RAM	1	12
INC DPTR	Increment Data Pointer	1	24
MUL AB	Multiply A and B	1	48
DIV AB	Divide A by B	1	48
DA A	Decimal Adjust Accumulator	1	12

LOGICAL OPERATIONS		Byte	Oscillator Period
ANL A,Rn	AND Register to Accumulator	1	12
ANL A,direct	AND direct byte to Accumulator	2	12
ANL A,@Ri	AND indirect RAM to Accumulator	1	12
ANL A,#data	AND immediate data to Accumulator	2	12
ANL direct,A	AND Accumulator to direct byte	2	12
ANL direct,#data	AND immediate data to direct byte	3	24
ORL A,Rn	OR register to Accumulator	1	12
ORL A,direct	OR direct byte to Accumulator	2	12
ORL A,@Ri	OR indirect RAM to Accumulator	1	12
ORL A,#data	OR immediate data to Accumulator	2	12
ORL direct,A	OR Accumulator to direct byte	2	12
ORL direct,#data	OR immediate data to direct byte	3	24
XRL A,Rn	Exclusive-OR register to Accumulator	1	12
XRL A,direct	Exclusive-OR direct byte to Accumulator	2	12
XRL A,@Ri	Exclusive-OR indirect RAM to Accumulator	1	12
XRL A,#data	Exclusive-OR immediate data to Accumulator	2	12
XRL direct,A	Exclusive-OR Accumulator to direct byte	2	12
XRL direct,#data	Exclusive-OR immediate data to direct byte	3	24
CLR A	Clear Accumulator	1	12
CPL A	Complement Accumulator	1	12
RL A	Rotate Accumulator left	1	12
RLC A	Rotate Accumulator left through the carry	1	12
RR A	Rotate Accumulator right	1	12
RRC A	Rotate Accumulator right through the carry	1	12
SWAP A	Swap nibbles within the Accumulator	1	12

DATA TRANSFER		Byte	Oscillator Period
MOV A,Rn	Move register to Accumulator	1	12
MOV A,direct	Move direct byte to Accumulator	2	12
MOV A,@Ri	Move indirect RAM to Accumulator	1	12
MOV A,#data	Move immediate data to Accumulator	2	12
MOV Rn,A	Move Accumulator to register	1	12
MOV Rn,direct	Move direct byte to register	2	24
MOV RN,#data	Move immediate data to register	2	12
MOV direct,A	Move Accumulator to direct byte	2	12
MOV direct,Rn	Move register to direct byte	2	24
MOV direct,direct	Move direct byte to direct	3	24
MOV direct,@Ri	Move indirect RAM to direct byte	2	24
MOV direct,#data	Move immediate data to direct byte	3	24
MOV @Ri,A	Move Accumulator to indirect RAM	1	12
MOV @Ri,direct	Move direct byte to indirect RAM	2	24
MOV @Ri,#data	Move immediate data to indirect RAM	2	12
MOV DPTR,#data16	Load Data Pointer with a 16-bit constant	3	24
MOVC A,@A+DPTR	Move Code byte relative to DPTR to ACC	1	24
MOVC A,@A+PC	Move Code byte relative to PC to ACC	1	24
MOVX A,@Ri	Move external RAM (8-bit addr) to ACC	1	24
MOVX A,@DPTR	Move external RAM (16-bit addr) to ACC	1	24
MOVX A,@Ri,A	Move ACC to external RAM (8-bit addr)	1	24
MOVX @DPTR,A	Move ACC to external RAM (16-bit addr)	1	24
PUSH direct	Push direct byte onto stack	2	24
POP direct	Pop direct byte from stack	2	24
XCH A,Rn	Exchange register with Accumulator	1	12
XCH A,direct	Exchange direct byte with Accumulator	2	12
XCH A,@Ri	Exchange indirect RAM with Accumulator	1	12
XCHD A,@Ri	Exchange low-order digit indirect RAM with ACC	1	12

BOOLEAN VARIABLE MANIPULATION		Byte	Oscillator Period
CLR C	Clear carry	1	12
CLR bit	Clear direct bit	2	12
SETB C	Set carry	1	12
SETB bit	Set direct bit	2	12
CPL C	Complement carry	1	12
CPL bit	Complement direct bit	2	12
ANL C,bit	AND direct bit to carry	2	24
ANL C,/bit	AND complement of direct bit to carry	2	24
ORL C,bit	OR direct bit to carry	2	24
ORL C,/bit	OR complement of direct bit to carry	2	24
MOV C,bit	Move direct bit to carry	2	12
MOV bit,C	Move carry to direct bit	2	24
JC rel	Jump if carry is set	2	24
JNC rel	Jump if carry not set	2	24
JB rel	Jump if direct bit is set	3	24
JNB rel	Jump if direct bit is not set	3	24
JBC bit,rel	Jump if direct bit is set and clear bit	3	24

PROGRAM BRANCHING		Byte	Oscillator Period
ACALL addr11	Absolute subroutine call	2	24
LCALL addr16	Long subroutine call	3	24
RET	Return from subroutine	1	24
RETI	Return from interrupt	1	24
AJMP addr11	Absolute jump	2	24
LJMP addr16	Long jump	3	24
SJMP rel	Short jump (relative addr)	2	24
JMP @A+DPTR	Jump indirect relative to the DPTR	1	24
JZ rel	Jump if Accumulator is zero	2	24
JNZ rel	Jump if Accumulator is not zero	2	24
CJNE A,direct,rel	Compare direct byte to ACC and jump if not equal	3	24
CJNE A,#data,rel	Compare immediate to ACC and jump if not equal	3	24
CJNE RN,#data,rel	Compare immediate to register and jump if not equal	3	24
CJNE @Ri,#data,rel	Compare immediate to indirect and jump if not equal	3	24
DJNZ Rn,rel	Decrement register and jump if not zero	2	24
DJNZ direct,rel	Decrement direct byte and jump if not zero	3	24
NOP	No operation	1	12

INSTRUCTIONS THAT AFFECT FLAG SETTING

	C	OV	AC
ADD	X	X	X
ADDC	X	X	X
SUBB	X	X	X
MUL	0	X	
DIV	0	X	
DA	X		
RRC	X		
RLC	X		

	C	OV	AC
CLR C	0		
CPL C	X		
ANL C,bit	X		
ANL C,/bit	X		
ORL C,bit	X		
ORL C,/bit	X		
MOV C,bit	X		
CJNE	X		
SETB C	1		

8051 COMMON INSTRUCTIONS

ADD A,<src-byte>
ADD adds the byte variable indicated to the Accumulator, leaving the result in the Accumulator. The carry and auxiliary-carry flags are set, respectively, if there is a carry-out from bit 7 or bit 3, and cleared otherwise. When adding unsigned integers, the carry flag indicates an overflow occurred. OV is set if there is a carry-out of bit 6 but not out of bit 7, or a carry-out of bit 7 but not bit 6; otherwise OV is cleared. When adding signed integers, OV indicates a negative number produced as the sum of two positive operands, or a positive sum from two negative operands. Four source operand addressing modes are allowed: register, direct, register-indirect, or immediate.

Examples:

ADD A,Rn (A) ← (A) + (Rn)

ADD A,Direct (A) ← (A) + (Direct)

ADD A,@Ri (A) ← (A) + ((Ri))

ADD A,#Data (A) ← (A) + #Data

SUBB A, <src-byte>
SUBB subtracts the indicated variable and the carry flag together from the Accumulator, leaving the result in the Accumulator. SUBB sets the carry (borrow) flag if a borrow is needed for bit 7, and clears C otherwise. (If C was set before executing a SUBB instruction, this indicates that a borrow was needed for the previous step in a multiple precision subtraction, so the carry is subtracted from the Accumulator along with the source operand.) AC is set if a borrow is needed for bit 3, and cleared otherwise. OV is set if a borrow is needed into bit 6, but not into bit 7, or into bit 7, but not bit 6. When subtracting signed integers OV indicates a negative number produced when a negative value is subtracted from a positive value, or a positive result when a positive number is subtracted from a negative number.

Examples:

SUBB A,Rn (A) ← (A) – (C) – (Rn)

SUBB A,Direct(A) ← (A) – (C) – (Direct)

SUBB A,@RI (A) ← (A) – (C) – ((Ri))

SUBB A,#Data (A) ← (A) – (C) - #Data

DIV AB
DIV AB divides the unsigned eight-bit integer in the Accumulator by the unsigned eight-bit integer in register B. The Accumulator receives the integer part of the quotient; register B receives the integer remainder. The carry and OV flags will be cleared.

MUL AB
MUL AB multiplies the unsigned eight-bit integers in the Accumulator and register B. The low-order byte of the sixteen-bit product is left in the Accumulator, and the high-order byte in B. If the product is greater than 255 (0FFH) the overflow flag is set; otherwise it is cleared. The carry flag is always cleared.

MOVC A,@A+<base-reg>
The MOVC instructions load the Accumulator with a code byte, or constant from program memory. The address of the byte fetched is the sum of the original unsigned eight-bit Accumulator contents and the contents of a sixteen-bit base register, which may be either the Data Pointer or the PC. In the latter case, the PC is incremented to the address of the following instruction before being added with the Accumulator; otherwise the base register is not altered. Sixteen-bit addition is performed so a carry-out from the low-order eight bits may propagate through higher-order bits. No flags are affected.

Example:

MOVC A,@A+DPTR: (A) ← ((A) + (DPTR))

LCALL addr16
LCALL calls a subroutine located at the indicated address. The instruction adds three to the program counter to generate the address of the next instruction and then pushes the 16-bit result onto the stack (low byte first), incrementing the Stack Pointer by two. The high-order and low-order bytes of the PC are then loaded, respectively, with the second and third bytes of the LCALL instruction. Program execution continues with the instruction at this address. The subroutine may therefore begin anywhere in the full 64k-byte program memory address space. No flags are affected.

RET
RET pops the high- and low-order bytes of the PC successively from the stack, decrementing the Stack Pointer by two. Program execution continues at the resulting address, generally the instruction immediately following an ACALL or LCALL. No flags are affected.

POP Direct
The contents of the internal RAM location addressed by the Stack Pointer is read, and the Stack Pointer is
decremented by one. The value read is then transferred to the directly addressed byte indicated. No flags are affected.

PUSH Direct
The Stack Pointer is incremented by one. The contents of the indicated variable is then copied into the internal RAM location addressed by the Stack Pointer. Otherwise no flags are affected.

ANL <dest-byte>,<src-byte>
ANL performs the bitwise logical-AND operation between the variables indicated and stores the results in the destination variable. No flags are affected. The two operands allow six addressing mode combinations. When the destination is the Accumulator, the source can use register, direct, register-indirect, or immediate addressing; when the destination is a direct
address, the source can be the Accumulator or immediate data.

ORL <dest-byte>,<src-byte>
ORL performs the bitwise logical-OR operation between the indicated variables, storing the results in the destination byte. No flags are affected. The two operands allow six addressing mode combinations. When the destination is the Accumulator, the source can use register, direct, register-indirect, or immediate addressing; when the destination is a direct address, the source can be the Accumulator or immediate data.

JB bit,rel
If the indicated bit is a one, jump to the address indicated; otherwise proceed with the next instruction. The branch destination is computed by adding the signed relative-displacement in the third instruction byte to the PC, after incrementing the PC to the first byte of the next instruction. The bit tested is not modified. No flags are affected.

JNZ rel
If any bit of the Accumulator is a one, branch to the indicated address; otherwise proceed with the next instruction. The branch destination is computed by adding the signed relative-displacement in the second nstruction byte to the PC, after incrementing the PC twice. The Accumulator is not modified. No flags are affected.

JZ rel
If all bits of the Accumulator are zero, branch to the indicated address; otherwise proceed with the next instruction. The branch destination is computed by adding the signed relative-displacement in the second instruction byte to the PC, after incrementing the PC twice. The Accumulator is not modified. No flags are affected.

DJNZ <byte>,<rel-addr>
DJNZ decrements the location indicated by 1, and branches to the address indicated by the second operand if the resulting value is not zero. An original value of 00H will underflow to 0FFH. No flags are affected. The branch destination would be computed by adding the signed relative-displacement value in the last instruction byte to the PC, after incrementing the PC to the first byte of the following instruction. The location decremented may be a register or directly addressed byte.

CJNE <dest-byte>,<src-byte>,rel
CJNE compares the magnitudes of the first two operands, and branches if their values are not equal. The branch destination is computed by adding the signed relative-displacement in the last instruction byte to the PC, after incrementing the PC to the start of the next instruction. The carry flag is set if the unsigned integer value of <dest-byte> is less than the unsigned integer value of <src-byte>; otherwise, the carry is cleared. Neither operand is affected.

The first two operands allow four addressing mode combinations: the Accumulator may be compared with any directly addressed byte or immediate data, and any indirect RAM location or working register can be compared with an immediate constant.

RL A
The eight bits in the Accumulator are rotated one bit to the left. Bit 7 is rotated into the bit 0 position. No flags are affected.

RLC A
The eight bits in the Accumulator and the carry flag are together rotated one bit to the left. Bit 7 moves into the carry flag; the original state of the carry flag moves into the bit 0 position. No other flags are affected.